Curriculum Vitae – Daniele Ielmini

Present Position

Assistant Professor
Dipartimento di Elettronica e Informazione
Politecnico di Milano
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Previous positions

2006	Visiting Scientist, Intel Corporation and CIS – Stanford University
2000 – 2002	Research Assistant, Dipartimento di Elettronica e Informazione, Politecnico di Milano

Education

1997 – 2000	Ph.D., Nuclear Engineering, Politecnico di Milano
1989 – 1995	Laurea, Nuclear Engineering, Politecnico di Milano

Awards

2007	Impressive Award for Best Presentation at the European Phase Change and Ovonic Science Symposium, E/PCOS 2007

Conference Organizations

2006 – 2008	International Reliability Physics Symposium (IRPS), Subcommittee Member for Dielectrics and Memory
2007	International Reliability Physics Symposium (IRPS), Workshop organizer and moderator for Non volatile memory
2008 – 2009	International Electron Device Meeting (IEDM), Subcommittee Member for Memory Technology and Session Co-chair
2008 – 2009	Semiconductor Interface Specialist Conference (SISC), Member of the Technical Committee and Session Chair
2009	Insulating Films on Semiconductors (INFOS), Session Chair
2009	International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Session Chair

Instructor

2008	Tutorial on Non Volatile Memories, International Reliability Physics Symposium (IRPS)
2007	Tutorial on Memory Reliability, International Reliability Physics Symposium (IRPS)
2005	Tutorial on Memory Reliability, International Reliability Physics Symposium (IRPS)

Teaching Experiences

2002 – 2009	Solid State Electronics, Undergraduate Student Course, EE, Politecnico di Milano (http://corsi.dei.polimi.it/ess/)
2006 – 2008	Nonvolatile Memories, Graduate Student Course, EE, Politecnico di Milano
2000 – 2008	Fundamental of Electronics, Undergraduate Student Course, EE, Politecnico di Milano
2008	Nonvolatile Resistive Memories, Graduate Students Course, Master in Technologies for Micro-Nano Electronics, Università della Sapienza, Roma

Journal Reviewer

Applied Physics Letters, Journal of Applied Physics, IEEE Transaction on Electron Devices, IEEE Electron Device Letters, Semiconductor Science and Technology, Journal of Non-Crystalline Solids, Microelectronic Engineering, Journal of Physics C

Professional Memberships

Institute of Electrical and Electronics Engineers (IEEE)
Material Research Society (MRS)

General Research Interests

Research interests fall in the realm of CMOS and post-CMOS devices and circuits, particularly regarding the characterization and modeling of memory devices and their scaling challenges. My past research activity has been devoted to the following topics:

- CMOS front-end reliability (leakage currents, hot carrier effects, NBTI)
- Modeling and characterization of CMOS-based non volatile memories (Flash, nanocrystal, charge trap memories)
- Modeling and characterization of emerging non volatile memories (phase change memory – PCM, resistive switching memory – RRAM)

Ph.D./Postdoc Student Supervisor

Christian Monzio Compagnoni (Ph.D., 2005, now Assistant Professor at PoliMi)
Deepak Sharma (Post doc, 2006 – 2008, now with EPFL – Lausanne)
Davide Mantegazza (MS 2004, Ph.D. 2008, now with Intel Corporation)
Ugo Russo (MS 2005, Ph.D. 2009, now with CNR-MDM Laboratories)
Simone Lavizzari (MS 2006, Ph.D. expected in 2010)
Carlo Cagli (MS 2007, Ph.D. expected in 2011)
Davide Fugazza (Ph.D. expected in 2011)
Federico Nardi (MS 2008, Ph.D. expected in 2012)

Invited seminars

- "Characterization and modeling of stress induced leakage currents in thin gate dielectrics," STMicroelectronics, Agrate Brianza, Italy, Feb. 11, 2000.
- "Characterization and modeling of SILC in MOSFETs and memories," Università La Sapienza, Roma, Italy, Oct. 8, 2001.
- "Characterization, modeling and prediction of data retention for Flash memories," STMicroelectronics, Agrate Brianza, Italy, Nov. 22, 2002.
- "Understanding data loss in Flash memories, characterization methods and physical mechanisms," STMicroelectronics, Agrate Brianza, Italy, Mar. 10, 2005.
- "Phase change memory characterization and modeling: data retention and recovery behavior," Stanford University, Stanford, CA, USA, Dec. 9, 2005.
- "Physical modeling of threshold switching in chalcogenide glasses," RWTH Aachen, Apr. 12, 2007.
- "Electrical modeling of material and cell behavior in phase change memories," Numonyx, Agrate Brianza, Italy, Jul. 5, 2007.
- "Conduction mechanisms and threshold switching in amorphous chalcogenide phase change materials," Dipartimento di Fisica, Università di Modena, Italy, Nov. 23, 2007.
- "Resistive-switching materials and memories," Inter-University Nano-Electronic Team, Bertinoro, Italy, Nov. 24, 2007.
- "PCM electrical characterization and reliability," Numonyx, Agrate Brianza, Italy, Jul. 21, 2008.
- "Physical mechanism and modeling of threshold switching in PCM cells," Intel Corporation, Santa Clara, CA, USA, Aug. 1, 2008.
- "Reset current scaling and reliability trends in phase change memory," Numonyx, Agrate Brianza, Italy, Nov. 18, 2008.
- "Physical modeling of electrical conduction and switching in phase change memories," Intel Corporation, Santa Clara, CA, USA, Dec. 18, 2008.
- "Physical mechanism and modeling of resistance switching in metal-oxide resistive memory (RRAM) devices," Lawrence Berkeley National Laboratories, Berkeley, CA, USA, Dec. 19, 2008.
- "Unified view into structural relaxation and crystallization in phase change memories," Intel Corporation, Santa Clara, CA, USA, Apr. 22, 2009.
- "Modeling resistance switching in metal oxide and chalcogenide materials," Hewlett-Packard Labs, Palo Alto, CA, USA, Apr. 24, 2009.
- "Reliability and scaling challenges of phase-change memories from a physical-modeling perspective," Samsung Electronics, Giheon, South Korea, Jul. 22, 2009.
- "Reliability and scaling challenges of phase-change memories from a physical-modeling perspective," Hynix, Ichon, South Korea, Jul. 23, 2009.
- "Reliability and scaling challenges of phase-change memories from a physical-modeling perspective," Korea Institute for Science and Technology, KIST, Seoul, South Korea, Jul. 23, 2009.
- "Distributed Poole-Frenkel conduction in amorphous phase change materials," Intel Corporation, Santa Clara, CA, USA, Sept. 8, 2009.

Patents

[1] A. Visconti, M. Bonanomi, D. Ielmini and A. S. Spinelli, "Method for programming/erasing a non volatile memory cell device, in particular for flash type memories," European Patent EP 1 833 058 A1, United States Patent Application US 2007/0211534 A1.

Book Chapters

[2] D. Ielmini, "Phase change memory device modeling," in Phase Change Materials – Science and Applications, S. Raoux and M. Wuttig Eds., 299-330 (2009). ISBN 978-0-387-84873-0.

[3] C. Monzio Compagnoni, R. Gusmeroli, A. S. Spinelli, D. Ielmini, A. L. Lacaita and A. Visconti, "Present status and scaling challenges for the NOR Flash memory technology," in Solid State Electronics Research Advances, Sergo Kobacze ed., 101-134 (2009). ISBN 978-1-60021-851-4

Invited Papers in Journals and Conference Proceedings

[4] A. Pirovano, A. Redaelli, F. Pellizzer, F. Ottogalli, M. Tosi, D. Ielmini, A. L. Lacaita and R. Bez, "Reliability study of phase-change non-volatile memories," IEEE Trans. on Device and Material Reliability 4, 422-427 (2004).
[5] D. Ielmini, A. S. Spinelli and A. L. Lacaita, "Recent developments on Flash memory reliability," Proc. INFOS 2005, published on special issue of Microelectron. Eng. 80C, 321-328 (2005).
[6] C. Monzio Compagnoni, R. Gusmeroli, D. Ielmini, A. S. Spinelli, A. L. Lacaita, "Silicon nanocrystal memories: a status update," Journal of Nanoscience and Nanotechnology 7, 193-205 (2007).
[7] D. Ielmini and A. L. Lacaita, "Physical modeling of conduction and switching mechanisms in phase change memory cells," European Phase Change and Ovonics Science Symposium, E*PCOS (2007).
[8] A. L. Lacaita and D. Ielmini, "Status and challenges of phase change memory modeling," European Solid-State Device Research Conference, ESSDERC, 214-221 (2007).
[9] A. L. Lacaita and D. Ielmini, "Reliability issues and scaling projections for phase change non volatile memories," IEDM Tech. Dig.,157-160 (2007).
[10] A. L. Lacaita, U. Russo and D. Ielmini, "Recent advances on the modeling of phase change materials and devices," Mater. Res. Soc. Symp. Proc. 1072-G06-05 (2008).
[11] D. Ielmini, "Modeling of switching phenomena in phase-change memory (PCM) devices," 99-106, European Phase-Change and Ovonic Symposium (E*PCOS), Prague, Czech Republic, Sept. 7-9, 2008.
[12] D. Ielmini, "Reliability issues and modeling of Flash and post-Flash memory," Insulating Films on Semiconductors – INFOS, Cambridge, UK (June 2009), also appearing in Microelectron. Eng. 86, 1870-1875 (2009).
[13] D. Ielmini, "Reliability and scaling challenges of phase-change memories from a physical-modeling perspective," 4th International Symposium on Next-generation Non-volatile Memory Technology for Terabit Memory, Seoul, Korea, July 24, 2009.
[14] D. Ielmini, "Phase change memory scaling from a reliability modeling perspective," International Workshop on Emerging Nonvolatile Memories, Satellite Workshop of IEEE Nano, Genova, Italy, Jul. 31, 2009.
[15] D. Ielmini, "Overview of modeling approaches for scaled non volatile memories," International Conference on Simulation of Semiconductor Processes and Devices, SISPAD, San Diego, CA, USA, Sept. 9-11, 2009.
[16] A. L. Lacaita and D. Ielmini, "Bridging carrier transport and amorphous dynamics in phase change materials," Proceedings of the 2009 European Phase-Change and Ovonic Symposium (E*PCOS), 2009.
[17] D. Ielmini, "Modeling of resistance switching and reliability in non volatile PCM and RRAM," International Symposium on Integrated Ferroelectrics and Functionalities, ISIF2, Colorado Springs, CO, Sept. 27 – Oct. 1, 2009.
[18] S. Raoux, W. Welnic and D. Ielmini, "Phase change materials and their application to non-volatile memories," Chemical Review (2009). In press, doi: 10.1021/cr900040x.
[19] D. Ielmini, "A unified physical picture of reliability mechanisms in phase change memory," Current Applied Physics (2009). In press.
[20] D. Ielmini, "Unified physical interpretation of instability mechanisms in phase-change materials," MRS Spring Meeting, San Francisco, April 5-9, 2010.

Tutorial Talks

[21] A. S. Spinelli and D. Ielmini, "A physical look at some reliability aspects of NOR Flash memories", IRPS Tutorial (2005).
[22] D. Ielmini, "Memory Reliability Year-in Review," IRPS Review (2007).
[23] D. Ielmini, "Physical mechanisms and modeling of Flash and post-Flash reliability," IRPS Tutorial (2008).

International Refereed Journals

[24] G. Ghislotti, D. Ielmini, E. Riedo, M. Martinelli and M. Dellagiovanna, "Picosecond time-resolved luminescence studies of recombination processes in CdTe," Solid State Commun. 111, 211-216 (1999).
[25] G. Ghislotti, E. Riedo, D. Ielmini and M. Martinelli, "Intersubband relaxation time for $In_xGa_{1-x}As$/AlAs quantum wells with large transition energy," Appl. Phys. Lett. 75, 3626-3628 (1999)
[26] A. S. Spinelli, A. L. Lacaita, M. Rigamonti, D. Ielmini and G. Ghidini, "Separation of electron and hole traps by transient current analysis," Microelectron. Eng. 48, 151-154 (1999).
[27] D. Ielmini, A. S. Spinelli and A. L. Lacaita, "Experimental evidence for recombination-assisted leakage in thin oxides," Appl. Phys. Lett. 76, 1719-1721 (2000)
[28] D. Ielmini, A. S. Spinelli, A. L. Lacaita, A. Martinelli and G. Ghidini, "A recombination model for transient and stationary stress-induced leakage current," Microelectron. Reliab. 40, 703-706 (2000)
[29] D. Ielmini, A. S. Spinelli, M. A. Rigamonti and A. L. Lacaita, "Modeling of SILC based on electron and hole tunneling - Part I: Transient effects," IEEE Trans. Electron Devices 47, 1258-1265 (2000)
[30] D. Ielmini, A. S. Spinelli, M. A. Rigamonti and A. L. Lacaita, "Modeling of SILC based on electron and hole tunneling - Part II: Steady-state," IEEE Trans. Electron Devices 47, 1266-1272 (2000)
[31] D. Ielmini, A. S. Spinelli, M. Beretta and A. L. Lacaita, "Different types of defect in the silicon dioxides characterized by their transient behavior," J. Appl. Phys. 89, 4189-4191 (2001)
[32] D. Ielmini, A. S. Spinelli, A. L. Lacaita, D. J. DiMaria and G. Ghidini "A Detailed investigation of the quantum yield experiment," IEEE Trans. Electron Devices 48, 1696-1702 (2001)
[33] D. Ielmini, A. S. Spinelli, A. L. Lacaita, A. Martinelli and G. Ghidini, "A recombination- and trap-assisted tunneling model for stress-induced leakage current," Solid State Electronics 45, 1361-1369 (2001)

[34] D. Ielmini, A. S. Spinelli, A. L. Lacaita and A. Modelli, “A new two-trap tunneling model for the anomalous SILC in flash memories,” Microelectron. Eng. 59, 189-195 (2001)
[35] D. Ielmini, A. S. Spinelli, A. L. Lacaita and A. Modelli, “Equivalent cell approach for extraction of the SILC distribution in Flash EEPROM cells,” IEEE Electron Device Lett. 23, 40-42 (2002)
[36] D. Ielmini, A. S. Spinelli, A. L. Lacaita and G. Ghidini, “Modeling of stress-induced leakage current and impact ionization in MOS devices,” Solid State Electronics 46, 417-422 (2002)
[37] D. Ielmini, A. S. Spinelli, A. L. Lacaita and A. Visconti, “Statistical profiling of SILC spot in Flash memories,” IEEE Trans. Electron Devices 49, 1723-1728 (2002)
[38] D. Ielmini, A. S. Spinelli, A. L. Lacaita and A. Modelli, “Modeling of anomalous SILC in Flash memories based on tunneling at multiple defects,” Solid State Electronics 46, 1749-1756 (2002)
[39] D. Ielmini, A. S. Spinelli, A. L. Lacaita and A. Modelli, “A statistical model for SILC in Flash memories,” IEEE Trans. Electron Devices 49, 1955-1961 (2002)
[40] G. Ghidini, A. Garavaglia, G. Giusto, A. Ghetti, R. Bottini, D. Peschiaroli, M. Scaravaggi, F. Cazzaniga and D. Ielmini, “Impact of gate stack process on conduction and reliability of 0.18um PMOSFET,” Microelectron. Reliab. 43, 1221-1227 (2003)
[41] C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli, A. L. Lacaita and C. Gerardi, “Study of nanocrystal memory reliability by CAST structures,” Solid-State Electronics 48, 1497-1502 (2004)
[42] D. Ielmini, A. L. Lacaita, A. Pirovano, F. Pellizzer and R. Bez, “Analysis of phase distribution in phase-change non volatile memories,” IEEE Electron Device Lett. 25, 507-509 (2004).
[43] D. Ielmini, A. S. Spinelli, A. L. Lacaita and M. J. van Duuren, “Defect generation statistics in thin gate oxides,” IEEE Trans. Electron Devices 51, 1288-1295 (2004).
[44] D. Ielmini, A. S. Spinelli, A. L. Lacaita and M. J. van Duuren, “Impact of correlated generation of oxide defects on SILC and breakdown distributions,” IEEE Trans. Electron Devices 51, 1281-1287 (2004).
[45] A. Redaelli, A. Pirovano, F. Pellizzer, A. L. Lacaita, D. Ielmini and R. Bez, “Electronic switching effect and phase-change transition in chalcogenide materials,” IEEE Electron Device Lett. 25, 684-686 (2004).
[46] D. Ielmini, A. S. Spinelli, A. L. Lacaita and M. J. van Duuren, “A comparative study of characterization techniques for oxide reliability in Flash memories,” IEEE Trans. on Device and Material Reliability 4, 320-326 (2004).
[47] G. Puzzilli, D. Caputo, F. Irrera, C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli, A. L. Lacaita and C. Gerardi, “Improving floating-gate memory reliability by nanocrystal storage and pulsed tunnel programming,” IEEE Trans. on Device and Material Reliability 4, 390-396 (2004).
[48] C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli and A. L. Lacaita, “Modeling of tunneling P/E for nanocrystal memories,” IEEE Trans. Electron Devices 52, 569-576 (2005).
[49] R. Gusmeroli, A. S. Spinelli, C. Monzio Compagnoni, D. Ielmini and A. L. Lacaita, “Edge and percolation effects on Vt window in nanocrystal memories,” Microelectronics Engineering 80, 186-189 (2005).
[50] D. Ielmini, D. Mantegazza, A. L. Lacaita, A. Pirovano and F. Pellizzer, “Parasitic reset in the programming transient of phase change memories,” IEEE Electron Device Lett. 26, 799-801 (2005).
[51] C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli and A. L. Lacaita, “Optimization of threshold voltage window under tunneling program/erase in nanocrystal memories,” IEEE Trans. Electron Devices 52, 2473-2481 (2005).
[52] D. Ielmini, D. Mantegazza, A. L. Lacaita, A. Pirovano and F. Pellizzer, “Switching and programming dynamics in phase change memory cells,” Solid-State Electronics 49, 1826-1832 (2005).
[53] D. Ielmini, A. S. Spinelli and A. Visconti, “Characterization of oxide trap energy by analysis of the SILC roll-off regime in Flash memories,” IEEE Trans. Electron Devices 53, 126-134 (2006).
[54] C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli and A. L. Lacaita, “Extraction of the floating-gate capacitive-couplings for drain turn-on estimation in discrete-trap memories,” Microelectron. Eng. 83, 319-322 (2006).
[55] D. Ielmini, A. Ghetti, A. S. Spinelli and A. Visconti, “A study of hot hole injection during programming drain disturb in Flash memories,” IEEE Trans. Electron Devices 53, 668-676 (2006).
[56] R. Gusmeroli, A. S. Spinelli, C. Monzio Compagnoni, and D. Ielmini, “Threshold-voltage statistics and conduction regimes in nanocrystal memories,” IEEE Electron Device Lett. 27, 409-411 (2006).
[57] U. Russo, D. Ielmini, A. Redaelli and A. L. Lacaita, “Intrinsic data retention in nanoscaled phase-change memories - Part I: Monte Carlo model for crystallization and percolation,” IEEE Trans. Electron Devices 53, 3032-3039 (2006).
[58] A. Redaelli, D. Ielmini, U. Russo and A. L. Lacaita, “Intrinsic data retention in nanoscaled phase-change memories - Part II: Statistical analysis and prediction of failure time,” IEEE Trans. Electron Devices 53, 3040-3046 (2006).
[59] D. Ielmini, A. L. Lacaita and D. Mantegazza, “Recovery and drift dynamics of resistance and threshold voltages in phase change memories,” IEEE Trans. Electron Devices 54, 308-315 (2007).
[60] D. Ielmini and Y. Zhang, “Evidence for trap-limited transport in the subthreshold conduction regime of chalcogenide glasses,” Appl. Phys. Lett. 90, 192102 (2007).
[61] D. Ielmini and Y. Zhang, “Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices,” J. Appl. Phys. 102, 054517 (2007).
[62] U. Russo, D. Ielmini and A. L. Lacaita, “Analytical modeling of chalcogenide crystallization for PCM data-retention extrapolation,” IEEE Trans. Electron Devices 54, 2769-2777 (2007).
[63] D. Mantegazza, D. Ielmini, A. Pirovano and A. L. Lacaita “Anomalous cells with low resistance in phase change memory arrays,” IEEE Electron Device Lett. 28, 865-867 (2007).
[64] U. Russo, D. Ielmini, A. Redaelli and A. L. Lacaita, “Modeling of programming and read performance in phase-change memories - Part I: Cell optimization and scaling,” IEEE Trans. Electron Devices 55, 506-514 (2008).
[65] U. Russo, D. Ielmini, A. Redaelli and A. L. Lacaita, “Modeling of programming and read performance in phase-change memories – Part II: program disturb and mixed scaling approach,” IEEE Trans. Electron Devices 55, 515-522 (2008).
[66] A. Redaelli, A. Pirovano, I. Tortorelli, D. Ielmini and A. L. Lacaita “A reliable technique for experimental evaluation of crystallization activation energy in PCMs,” IEEE Electron Device Lett. 29, 41-43 (2008).
[67] D. Mantegazza, D. Ielmini, A. Pirovano, A. L. Lacaita, E. Varesi, F. Pellizzer and R. Bez, “Explanation of programming distributions in phase-change memory arrays based on crystallization time statistics,” Solid-State Electronics. 52, 584-590 (2008).

[68] A. Redaelli, D. Ielmini, U. Russo and A. L. Lacaita "Modeling and simulation of conduction characteristics and programming operation in nanoscaled phase-change memory cells," J. Computational and Theoretical Nanoscience 5, 1183-1191 (2008).
[69] D. Ielmini, D. Mantegazza and A. L. Lacaita, "Voltage controlled relaxation oscillations in phase-change memory devices," IEEE Electron Device Lett. 30, 568-570 (2008).
[70] D. Ielmini, S. Lavizzari, D. Sharma and A. L. Lacaita, "Temperature acceleration of structural relaxation in $Ge_2Sb_2Te_5$," Appl. Phys. Lett. 92, 193511 (2008).
[71] D. Ielmini, "Threshold switching mechanism by high-field energy gain in the hopping transport of chalcogenide glasses," Phys. Rev. B 78, 035308 (2008).
[72] A. L. Lacaita, D. Ielmini and D. Mantegazza, "Status and challenges of phase change memory modeling," Solid-State Electronics 52, 1443-1451 (2008).
[73] U. Russo, D. Ielmini, C. Cagli and A. L. Lacaita, "Filament conduction and reset mechanism in NiO-based resistive-switching memory (RRAM) devices," IEEE Trans. Electron Devices 56, 186-192 (2009).
[74] U. Russo, D. Ielmini, C. Cagli and A. L. Lacaita, "Self-accelerated thermal dissolution model for reset programming in NiO-based resistive switching memory (RRAM) devices," IEEE Trans. Electron Devices 56, 193-200 (2009).
[75] M. Boniardi, A. Redaelli, A. Pirovano, I. Tortorelli, D. Ielmini and F. Pellizzer, "A physics-based model of electrical conduction decrease with time in amorphous $Ge_2Sb_2Te_5$," J. Appl. Phys. 105, 084506 (2009).
[76] U. Russo, D. Kalamanathan, D. Ielmini, A. L. Lacaita and M. Kozicki, "Study of multilevel programming in programmable metallization cell (PMC) memory," IEEE Trans. Electron Devices 56,1040-1047 (2009).
[77] D. Ielmini, C. Cagli and F. Nardi, "Resistance transition in metal oxides induced by electronic threshold switching," Appl. Phys. Lett. 94, 063511 (2009).
[78] D. Ielmini and M. Boniardi, "Common signature of many-body thermal excitation in structural relaxation and crystallization of chalcogenide glasses," Appl. Phys. Lett. 94, 091906 (2009).
[79] D. Ielmini, M. Boniardi, A. L. Lacaita, A. Redaelli and A. Pirovano, "Unified mechanisms for structure relaxation and crystallization in phase-change memory," Microelectron. Eng. 86, 1942-1945 (2009).
[80] D. Ielmini, D. Sharma, S. Lavizzari and A. L. Lacaita, "Reliability impact of chalcogenide-structure relaxation in phase change memory (PCM) cells – Part I: Experimental study," IEEE Trans. Electron Devices 56, 1070-1077 (2009).
[81] S. Lavizzari, D. Ielmini, D. Sharma and A. L. Lacaita, "Reliability impact of chalcogenide-structure relaxation in phase change memory (PCM) cells – Part II: Physics-based modeling," IEEE Trans. Electron Devices 56, 1078-1085 (2009).
[82] D. Kamalanathan, U. Russo, D. Ielmini, and M. N. Kozicki, "Voltage-driven ON-OFF transition and tradeoff with program and erase current in programmable metallization cell (PMC) memory," IEEE Electron Device Lett. 30, 553-555 (2009).
[83] D. Ielmini and F. Gattel, "Delay correction for accurate extraction of time exponent and activation energy of NBTI," IEEE Electron Device Lett. 30, 684-686 (2009).
[84] C. Cagli, F. Nardi and D. Ielmini, "Modeling of set/reset operations in NiO-based resistive-switching memory (RRAM) devices," IEEE Trans. Electron Devices 56, 1712-1720 (2009).
[85] D. Ielmini, M. Manigrasso, F. Gattel and G. Valentini, "A new NBTI model based on hole trapping and structure relaxation in MOS dielectrics," IEEE Trans. Electron Devices 56, 1943-1952 (2009).
[86] U. Russo, C. Cagli, S. Spiga, E. Cianci and D. Ielmini, "Impact of electrode materials on resistive-switching memory (RRAM) programmning," IEEE Electron Device Lett. 30, 817-819 (2009).

International Conference Proceedings

[87] M. Elena, D. Ielmini, A. Miotello and P. M. Ossi, "Structure and properties of sputter-deposited BN thin films," Elevated Temperature Coatings: Science and Technology II, TMS, N. B. Dahotre and J. M. Hampikian eds., 139-148 (1996). ISBN 0-87339-313-9
[88] G. Ghislotti, D. Ielmini, E. Riedo and M. Martinelli, "Picosecond time-resolved studies of defect-related recombination in high-resistivity CdTe, CdZnTe," Mat. Res. Soc. Symp. Proc., 510, 601-605 (1998). ISBN 1-55899-416-5
[89] D. Ielmini, A. S. Spinelli, A. L. Lacaita and G. Ghidini, "Impact ionization and stress-induced leakage current in thin gate oxides," Proc. ULIS 2000 Workshop, F. Balestra ed., 85-88 (2000). ISBN 2-9514840-0-3
[90] D. Ielmini, A. S. Spinelli, A. L. Lacaita and G. Ghidini, "Evidence for recombination at oxide defects and new SILC model," Proc. IRPS, 55-64 (2000). ISBN 0-7803-5860-0
[91] D. Ielmini, A. S. Spinelli, A. L. Lacaita and G. Ghidini, "Role of interface and bulk defect-states in the low-voltage leakage conduction of ultrathin oxides," Proc. Eur. Solid-State Device Res. Conf. 2000, Frontier Group, W. A. Lane et al. eds., 312-315 (2000). ISBN 2-86332-248-6
[92] D. Ielmini, A. S. Spinelli, A. L. Lacaita, D. J. DiMaria and G. Ghidini, "Experimental and numerical analysis of the quantum yield," IEDM Tech. Dig. 331-334 (2000). ISBN 0-7803-6438-4
[93] A. Modelli, F. Gilardoni, D. Ielmini and A. S. Spinelli "A new conduction mechanism for the anomalous bits in thin oxides Flash EEPROMs," Proc. IRPS, 61-66 (2001). ISBN 0-7803-6587-9
[94] D. Ielmini, A. S. Spinelli, A. L. Lacaita, L. Confalonieri and A. Visconti, "New technique for fast characterization of SILC distribution in Flash arrays," Proc. IRPS, 73-80 (2001). ISBN 0-7803-6587-9
[95] D. Ielmini, A. S. Spinelli, A. L. Lacaita and A. Modelli, "Statistical modeling of reliability and scaling projections for Flash memories," IEDM Tech. Dig. 703-706 (2001). ISBN 0-7803-7050-3
[96] D. Ielmini, A. S. Spinelli, A. L. Lacaita, R. Leone and A. Visconti, "Localization of SILC in Flash memories after program/erase cycling," Proc. IRPS, 1-6 (2002). ISBN 0-7803-7352-9
[97] D. Ielmini, A. S. Spinelli, A. Lacaita, M. Gubello and M. J. van Duuren, "Monitoring Flash EEPROM reliability by equivalent cell analysis," Proc. Eur. Solid-State Device Res. Conf. 2002, University of Bologna, G. Baccarani et al. eds., 359-362 (2002). ISBN 88-900847-8-2
[98] D. Ielmini, A. S. Spinelli, A. L. Lacaita and M. J. van Duuren, "Correlated defect generation in thin oxides and its impact on Flash reliability," IEDM Tech. Dig. 143-146 (2002). ISBN 0-7803-7462-2
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