Ph.D. in Information Technology
Thesis Defense

July 15th, 2025
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Room Beta – Building 24

Giacomo CASTORO – XXXVII Cycle

ADVANCES IN HIGH-SPECTRAL-PURITY LOCAL OSCILLATORS AND LOW-POWER FREQUENCY MODULATORS ENABLED BY DIGITALLY INTENSIVE FREQUENCY SYNTHESIZERS

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Abstract:

To meet the increasing demand for higher data rates, modern wireless transceivers (TRXs) are leveraging high-order quadrature amplitude modulation (QAM) schemes and multiple-input multiple-output (MIMO) operation at millimeter wave carrier frequencies while also maintaining low power consumption to maximize the battery life of portable devices. Additionally, they aim for minimal silicon area to reduce costs and enable more functionalities on the same IC. However, this approach imposes stricter requirements on the local oscillator (LO), particularly in terms of integrated jitter, settling time, spectral purity, and power dissipation.

The bang-bang phase-locked loop (BBPLL) architecture is an attractive option for LO implementation, offering lower power consumption and reduced area compared to other types of analog or digital phase-locked loop (PLL). This advantage stems from the use of a compact and efficient single bit quantizer for phase detection, known as the bang-bang phase detector (BBPD). However, the aggressive quantization performed by the BBPD significantly degrades the BBPLL's performance in terms of settling time, integrated jitter, and spurious tones, limiting its applicability in modern TRXs.

This thesis aims to demonstrate how the use of digital PLLs (DPLLs) for LO implementations can achieve spectral purity on par with that of analog PLLs while significantly reducing the overall footprint. Additionally, DPLLs provide the flexibility to introduce new functionalities within each PLL element with minimal area and power consumption. The goal of this research is to explore the potential of DPLLs in advanced communication systems, such as those that require low jitter (for example, 5G) or low power consumption (for example, BLE).

This thesis presents viable solutions to overcome the limitations of previous state-of-the-art DPLLs.

First, a BBPLL with a novel fractional spur reduction method is introduced. It is based on a multipath topology, where each path has its own digital-to-time converter (DTC) and phase detector (PD). We demonstrate that, by driving each DTC with appropriately shifted quantization error sequences and combining the PD outputs, the dominant fractional spurs caused by DTC nonlinearities can be canceled, resulting in a significant reduction in PLL jitter.

Second, a two-point modulated DPLL designed to support GFSK modulation for BLE packet transmission and adaptive frequency hopping (AFH) is presented. The two-point architecture allows

for a narrow bandwidth and low reference frequency, minimizing power dissipation while maintaining
a low FSK error. Additionally, the novel fast-locking technique introduced here effectively reduces the PLL frequency error when a frequency hop is applied.

PhD Committee

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