Ph.D. in Information Technology
Thesis Defenses

April 10th, 2025
At 10:30 a.m.
Room Alpha – Building 24

Matteo BALDO – XXXVI Cycle

NUMERICAL AND ANALYTICAL MODELING OF GE-RICH PHASE CHANGE MEMORY DEVICES
Supervisor: Prof. Daniele Ielmini

Abstract:

During the last decades, the world has seen a rapid change and capillary diffusion of electronic devices in every part of our life. From wearable electronics to smart devices passing through the thousands of sensors present nowadays in each new car and transportation vehicle; the amount of electronic devices around us has drastically risen.
This progress is fueled by the improvements of non-volatile memory storage capability. Each device has to have a small portion of data that should be conserved even when the system is powered off. Flash technology dominates the market in this field thanks to its reliability and scaling proprieties. During the last years this progress seems to have reached a halt. This is mainly due to physical reliability reasons that makes scaling the Flash memory cell a very strenuous task.
Is in this context, where large foundries are trying to develop alternative memory solutions with a high speed, large density, good scalability and reliability characteristics, that Phase Change Memory (PCM) devices have their role. These elements store the information in the atomic arrangement of the material (amorphous or crystalline) rather then the charge on a capacitor. This thesis will aims to explain and show different studies on the latest and most advanced PCM technology from STMicroelectronics; the embedded Ge-rich GST PCM.
Understanding the device physics is fundamental to predict and control the element behavior. In order to do this thorough analysis of electrical data was complemented with physical images such as Scanning Transition Electron Microscopy (STEM) or Electron Energy Loss Spectroscopy (EELS) to support the evidences. These data were used to create physics based modeling framework able to predict both electrical and physical evidences. The models shown range from a relatively simple analytical models to three dimensional thermo-electrical Technology Aided Computer Design (TCAD). Different tools for simulations were used from Comsol Multiphysics to the Synopsis Sentaurus suit passing through the development of some modules of Ginestra, the Applied Materials proprietary simulation software.
The device behaviors covered in this work permeate the memory life from production to application. The peculiar Ge-rich GST material evolution of the cells from process deposition to programming is shown considering both phase and composition. Time evolution of resistance level in the phenomena called drift with the complex temperature dependence and relation with crystallization. Applications of these devices to possible revolutionary new field such as Analog In-Memory Computing and evaluation of their perspective performances. This work is a product of the excellent collaboration between Politecnico di Milano and STMicroelectronics, in particular the Agrate PCM Excellence Center lead by Roberto Annunziata, that provided the data related to PCM devices.

Artëm GLUKHOV– XXXVII Cycle

DESIGN OF ENERGY-EFFICIENT NEURAL NETWORK ACCELERATORS WITH EMBEDDED PHASE CHANGE MEMORY DEVICES

Supervisor: Prof. Daniele Ielmini

Abstract:

AI and Neural networks are experiencing unrestricted growth in both public adoption and size. While we begin to glimpse the great capability, potential, and impact these algorithms may have on the social fabric of our times, a closer look shows that there is no free lunch in life, and the forever-growing neural network models hide in plain sight an unprecedented energy demand.

This novel, still evolving, and fastly growing computing application happens in conjunction with a constantly slowing evolution rate of traditional computing architectures. Among the many reasons behind this deceleration, the most evident are the (long) end of Moore's law, the rapidly increasing cost behind further technology node scaling, and an intrinsic difficulty in optimizing the traditional von Neumann architecture to the newly emerged data-intensive applications.

In this framework, the new paradigm of in-memory computing (IMC) finds its place as a promising candidate to complement the traditional architectures, accelerating those computations that are so expensive on typical machines yet so requested. IMC is made possible thanks to the flourishing research on emerging nonvolatile memory devices that can be organized in crosspoint arrays, memory matrices with high integration density, low- power, and highly parallel structures that enable trivial analog computation of matrix- vector multiplication, the main building blocks of the whole neural network framework.

As with almost everything in electronics, as we move further from an idea and get closer to a practical implementation, an infinite series of undesired and parasitic effects start polluting the outcome, complicating the task.

In-memory computing is not exempt from such problems, and indeed, between the nonide- alities of the memory devices, the circuital limitations, and the algorithmic compatibility issues, the task of developing a standard-setting and fully-featured IMC accelerator is still far from completion, despite the high amount of interest revolving around it.

In this scenario, this doctoral thesis ultimately focuses on the design and development of a fully-custom PCM-based ASIC for IMC acceleration, but before that, it retraces all the discussions and analysis starting from PCM devices and their programming algorithms, a differential readout scheme proposal that eventually has seen the light as another testchip, and the description of an analog-to-digital readout chain that was at the core of the last ASIC.

The research work tackled various challenges of the in-memory computing paradigm, exploring and addressing them from different standpoints, pivoting and exploiting the intrinsic multidisciplinarity of the field.

PhD Committee

Prof. Nicola Lusardi, **Politecnico di Milano**

Prof. David Esseni, **Università degli Studi di Udine**

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