Ph.D. in Information Technology
Thesis Defenses

March 6th, 2025
At 1:30 p.m.
Room Alpha – Building 24

Gabriele BE' – XXXVII Cycle

CALIBRATION TECHNIQUES IN RECONFIGURABLE TIME-INTERLEAVED ADCS
Supervisor: Prof. Salvatore Levantino

Abstract:

The demand for more connected devices, higher data rates, and lower-latency communications to enable next-generation applications has driven technological advancements in the last years, moving from the first-generation mobile networks to the fifth one (5G) and foreseeing the sixth generation in the near future. Each generation increases the data rate, introduces new features, adds flexibility to the standard, and improves performance. All these high-level aspects, defined in the communication standard, then translate to architecture and circuit-level requirements for the integrated circuits implementing the radio link. Wireless transceivers are incredibly complex systems that require detecting weak signals in the presence of strong interference. Analog-to-digital converters (ADCs) are critical components of the receiver chain, as they are placed at the boundary between the analog and the digital domain and are typically a performance bottleneck for the overall receiver chain. Modern communication standards targeting high bandwidths exploit, among others, wide channels, channel aggregation, and high-order modulation schemes, which translate to the ADC specifications. The 5G NR FR2 standard exploits wide channels at millimeter waves to avoid the crowded low-frequency spectrum and increase the data rate. Channels as large as 400 MHz, which extend to 1.2 GHz considering channel aggregation, demand for ADCs with sampling rates of a few GHz. Moreover, complex modulation schemes push for higher ADC resolutions with a sufficiently clean spectrum to avoid unwanted signals falling in the band of interest. This Ph.D. thesis discusses the concept, modeling, and practical design of time-interleaved (TI) ADCs targeting the 5G NR specifications. Time interleaving poses significant challenges to achieving the required performance due to sub-ADC mismatches, channel interactions, and the large front-end load. The techniques presented in this thesis allow overcoming these limitations, leading to a TI ADC with more than 9 bits of resolution at 2 GS/s with a high-frequency spurious-free dynamic range (SFDR) of about 70 dBc.

Paolo MELILLO – XXXVII Cycle

INTEGRATED DC-DC CONVERTERS WITH TIME-BASED CONTROL FOR PORTABLE AND INDUSTRIAL APPLICATIONS
Supervisor: Prof. Salvatore Levantino

Abstract:

The ever-increasing demand for high performance DC-DC converters with high efficiency, fast response, small area occupation and high switching frequency, is becoming difficult to meet with analog controllers. Time-based control has been demonstrated to be a preferable alternative to conventional analog and digital controllers, achieving fast transient response with reduced area occupation, as a result of the elimination of the power-hungry error-amplifier (EA) and of the pulse-width-modulator (PWM). Nevertheless, the lack of the PWM, commonly used to implement feedforward control and gain compensation, might be disadvantageous in some application scenarios. This thesis presents a buck converter and a boost converter with time-based control and different strategies to address the limitation induced by the absence of the PWM generator. The buck converter with 5 to 32V input voltage includes a novel PFM constant-charge control for light-load conditions and an adaptive gain time-based control with line feedforward. Thanks to the proposed techniques the converter shows a constant loop gain GBWP, the best line transient response and the minimum controller area of 0.31-mm2, when compared to wide-input-range converters. The boost converter for AMOLED applications comprises a novel time-based feedback PID (F-PID) which results in a convenient alternative to the conventional PID as it offers an additional path to exploit the line feedforward with negligible impact on the controller area occupation.
The proposed boost converter shows the best line transient performance and the minimum controller area of 0.21-mm2, when compared to the best state-of-the-art converters and available commercial products.

Luca RICCI – XXXVII Cycle

HIGH-SPEED SAR ADCS FOR TIME-INTERLEAVED DATA CONVERTERS
Supervisor: Prof. Andrea Giovanni Bonfanti

Abstract:

The widespread use of the Internet and the proliferation of connected devices have allowed us to experience a digital life alongside our analog one. This has been enabled through significant engineering efforts by the scientific and industrial communities to meet users' bandwidth demands. Recent wireless standards, such as the 5G New Radio (NR), have been developed for high speeds and efficient spectrum utilization. In this context, the analog-to-digital converter (ADC) is a critical player in receivers, serving as the bridge through which the analog information crosses towards the digital domain, where its processing occurs. Digital processing greatly benefits from technology scaling, which results in lower power consumption and higher speeds. Therefore, analog functions have progressively moved into the digital domain. This allows receivers to have less area since some

analog components can be removed from the signal acquisition chain. Additionally, the significant improvement of ADC performances in recent years has been instrumental in designing receivers capable of digitizing large bandwidth signals. This thesis focuses on ADCs for wireless applications requiring high speed and moderate resolution.
Achieving a GSps sampling rate with a single-channel ADC results in low energy efficiency, limited by the analog performance of transistors in CMOS technology. The time-interleaved architecture offers a viable solution by interleaving multiple ADCs. However, despite being an established architecture, it poses challenges to avoid degrading the single- channel performance when enabling the time-interleaving mode: driving a switched input impedance, inter-channel crosstalk, and sub-ADC mismatches. Moreover, the single- channel ADC needs to have a high sampling frequency to reduce the number of slices, thus reducing the effect of these issues. This work starts from the design of a single-channel ADC and arrives at the implementation of a TI converter during three projects. The SAR architecture is chosen among the possible ones for its energy efficiency and simplicity. The research focuses on optimizing its speed and linearity. The first project increases the SAR conversion robustness to settling errors employing three main techniques: redundancy, a full-custom unit capacitor for the capacitive digital-to-analog converter (CDAC), and a novel switching algorithm. The second project proposes a linearization technique for SAR ADCs to reduce the distortion caused by the non-linear comparator input capacitance. Finally, the last part of this thesis deals with the design of a 2-GSps TI ADC. It employs eight SAR ADCs equal to the second prototype. The issues in time-interleaved converters mentioned above are addressed as follows. First, an input buffer with improved high-frequency linearity drives the sub-ADC array. It reduces the distortion due to the inter-channel crosstalk through the input network. Second, each SAR ADC includes a reference voltage buffer that rejects supply and ground voltage disturbances, thus reducing the inter-channel crosstalk through the reference distribution network that degrades the converter resolution. Third, on-chip background calibrations mitigate the effect of sub-ADC mismatches. The converters are implemented in a 28-nm CMOS technology.
The first SAR ADC achieves a 150-MSps speed with a 10.2-ENOB resolution. It validates the proposed techniques, which results in good resolution and linearity compared to other SAR ADCs with similar sampling rates and resolutions. The second prototype achieves a sampling frequency of 250 MHz with an 11-bit resolution. After enabling the proposed linearization technique, measurement results show an increase of approximately 17 dB of the SAR ADC SFDR. This converter has been employed to implement the 2-GSps TI ADC. The measurement results show a 57.3-dB and a 70.1-dB SNDR and SFDR, respectively, close to the Nyquist frequency. The SNDR degrades by only 1.76 dB on a 1-GHz bandwidth, comparing the TI and single-channel ADC performances. It dissipates 118 mW, including input buffer and digital calibrations.

PhD Committee

Prof. Carlo Samori, **Politecnico di Milano**

Prof. Andrea Baschirotto, **Università degli Studi di Milano-Bicocca**

Prof. Stefano Saggini, **Università degli Studi di Udine**