Ph.D. in Information Technology
Thesis Defenses

September 6th, 2023
at 10:00
Room "Alpha"

Piergiulio Mannocci– XXXV Cycle
Analogue Circuit Design for In-Memory Linear Algebra Accelerators
Supervisor: Prof. **Daniele Ielmini**

Abstract:

Since its introduction in 1945, computing systems have been built around von Neumann's architecture, predicating the physical separation of memory and computing units on grounds of flexibility and generality. At the same time, Moore's law has dominated the scaling paradigm by predicting a yearly doubling in the number of transistors, consequently driving both academic and industrial efforts in the continuous miniaturization process. However, as data generation rates exceed the quintillion bytes per year and physical limits of complementary-metal-oxide-semiconductor (CMOS) technology mark the end of classical scaling, the increasingly data-driven workloads of modern-day applications exacerbate the energy and latency overheads associated with continuous data shuttling. In-memory computing (IMC) radically subverts the classical paradigm by performing computation in situ within the memory elements by exploiting physical laws, unlocking theoretically unrivaled throughput and energy efficiency improvements. Among the wide spectrum of proposed IMC architectures, closed-loop in-memory computing (CL-IMC) with emerging memory devices has attracted interest for its capability to accelerate computationally heavy operations of increasing use in artificial intelligence and machine learning, such as matrix inversion and linear regression.
This doctoral thesis focuses on the study, design, and testing of analog closed-loop circuits for in-memory accelerators. A complete mathematical theory for both static and dynamic properties of in-memory, linear matrix feedback circuits is rigorously derived and employed as the core engine of a matrix-based circuit simulator providing orders-of-magnitude speedups with respect to SPICE solvers. To expand the operational portfolio, several new circuits for the acceleration of regularized regressions, such as ridge and LASSO, matrix decomposition, and linear quadratic estimation, are introduced and characterized in terms of their accuracy and speed, demonstrating orders-of-magnitude improvement with respect to conventional digital solvers in selected applications including baseband processing in 6G communication systems, principal component analysis for data classification, and Kalman-filter-based sensor fusion. Experimental demonstrations on both CMOS-based systems and emerging-memory-based platforms complement the research work by providing real-world implementation of CL-IMC topologies and proving the feasibility of proposed solutions. The obtained results strengthen the position of CL-IMC as a promising candidate for next-genera□on energy-efficient algebraic accelerators.

PhD Committee
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