Ph.D. in Information Technology
Thesis Defenses

May 2nd, 2023
at 10:00
Room "Alpha" and online by Webex

Alessandro Dago– XXXIV Cycle
High Performance Resonant Switched Capacitor Converter (ReSCC) Topology for High Conversion Ratio DC-DC Voltage Conversion
Supervisor: Prof. **Salvatore Levantino**

Abstract:

In recent years, resonant switched-capacitor converters (ReSCC) proved to be a valid alternative to traditional buck converters, thanks to their key features such as very high power density, high efficiency, and capability of adjusting the output voltage through quasi-resonant operation. However, since the components count increases with the conversion ratio, these advantages are usually limited to ReSCC topologies providing 2-to-1 nominal down-conversion. This thesis presents a novel DC-DC ReSCC topology derived from ladder structure with reduced number of components for nominal 4-to-1 voltage conversion. Two converters have been implemented to validate the proposed topology, the first one is an integrated solution to perform 12 V to PoL down-conversion. A novel control system for 3-phase quasi-resonant output voltage regulation has been introduced to regulate the output voltage in the 2.5 to 3 V output voltage range. Thanks to the employment of parasitic PCB inductors, a peak power density of 0.53 W/mm2 is reached, while a peak closed loop efficiency of 94.4 % has been measured. The second application is a discrete components unregulated 48 V bus converter, which makes use of a custom planar multi-tapped autotransformer to perform a direct down conversion toward 3.4 V (14-to-1 conversion ratio). A 415 W/inch3 has been obtained at 140 A output current, corresponding to 440 W delivered output power.
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Simone Mattia Dartizio- XXXV Cycle
Design of Small-Footprint, High-Spectral Purity and Low-Jitter Digitally-Intensive Frequency Synthetizers
Supervisor: Prof. **Salvatore Levantino**

Abstract:

To substain the pervasive expansion of mobile data networks of the last decades, modern wireless transceivers (TRXs) are required to achieve wide data-rates, while at the same time featuring a low power consumption to avoid limiting the lifetime of battery-powered devices and a low silicon area occupation to reduce their cost and therefore provide more functionalities on the same IC. One of the most critical TRX blocks is the local oscillator (LO), which performance in terms of integrated jitter, settling-time and spectral purity greatly affect the TRX operation. The bang-bang phase-locked-loop (BBPLL) architecture is a promising candidate for the LO implementation, due to its

lower power consumption and area occupation when compared to other types of either analog or digital phase-locked loops (PLLs), thanks to the compact and efficient single-bit quantizer employed for phase-detection, denoted as bang-bang phase-detector (BBPD). However, due to the strong quantization operated by the BBPD, the BBPLL performance in terms of settling time, integrated jitter and spurious tones are highly degraded, thus preventing the use of BBPLLs in modern TRXs. In this thesis, three viable solutions to overcome the limitations of BBPLLs are presented. First, a BBPLL employing a novel single-bit noise shaping phase detector, denoted as S-BBPD, allows to overcome the quantization noise limitation of conventional BBPLL architectures, thus bridging the performance gap which exists between BBPLLs and analog PLLs. An adaptive algorithm, working in the background of the main system, optimizes the performance of the S-BBPD across process, voltage and temperature (PVT) variations. Second, a BBPLL employing two novel fast-locking techniques breaking the strong jitter vs locking time trade-off typical of BBPLL architectures is presented. The first technique guarantees the absence of limit cycles within the PLL transient and optimizes the PLL settling time. The second technique allows to reduce the PLL frequency error upon the application of a frequency jump. Third, a BBPLL employing two novel fractional spur reduction solutions is presented. The first is based on the use of a novel highly linear digital-to-time converter (DTC) architecture. The second is based on a novel quantization error (Q-error) randomization technique allowing to scramble the Q-error without requiring to increase the DTC range and thus the PLL jitter - a problem currently shared by state-of-the-art Q-error randomization techniques.

PhD Committee
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